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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/066,475	02/01/2002	Edward Colles Nevill	1103179-0009	5943

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PATENT DEPARTMENT
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EXAMINER	
COULTER, KENNETH R	
ART UNIT	**PAPER NUMBER**
2141	

DATE MAILED: 02/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/066,475	NEVILL, EDWARD COLLES	
	Examiner	Art Unit	
	Kenneth R. Coulter	2141	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-70* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-70* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Reissue Applications

1. Applicant is reminded of the continuing obligation under 37 CFR 1.178(b), to timely apprise the Office of any prior or concurrent proceeding in which Patent No. 6,021,265 is or was involved. These proceedings would include interferences, reissues, reexaminations, and litigation.

Applicant is further reminded of the continuing obligation under 37 CFR 1.56, to timely apprise the Office of any information which is material to patentability of the claims under consideration in this reissue application. These obligations rest with each individual associated with the filing and prosecution of this application for reissue. See also MPEP §§ 1404, 1442.01 and 1442.04.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 – 70 are rejected under 35 U.S.C. 102(b) as being anticipated by Larsen (U.S. Pat. No. 5,115,500) (Plural Incompatible Instruction Format Decode Method and Apparatus).

3.1 Regarding claim 1, Larsen discloses a data processing apparatus comprising:

(a) a processor core operable to execute successive program instruction words of a predetermined plurality of instruction sets stored in a data memory (Abstract; Figs. 1A, 1B, 2; col. 3, lines 15 - 43);

(b) a program counter register for indicating an address of a next program instruction word in said data memory (Fig. 2, item 3 "IAR"; Fig. 1A, item 3 "IAR"; col. 3, lines 59 - 62);

(c) logic operable to modify the contents of said program counter register in response to a current program instruction word (Figs. 1A, 2; col. 3, lines 31 – 43; col. 3, line 52 – col. 4, line 6; Additionally, it was well known in the art that a program counter in a microprocessor has a program counter register modifier.);

(d) a processor core controller, responsive to one or more predetermined indicator bits of said program counter register, operable to control said processor core to execute program instruction words of a current instruction set selected from said predetermined plurality of instruction sets and specified by the state of said one or more indicator bits of said program counter register (Fig. 2; col. 5, line 34 – col. 6, line 2);

(e) a memory access controller operable to access program instruction words stored in said data memory, said access controller not being responsive to said one or more indicator bits of said program counter register (Fig. 2; col. 5, line 34 – col. 6, line 2).

3.2 Per claim 2, Larsen teaches the following additional features:

a first instruction decoder for decoding program instruction words of a first instruction set (Fig. 1A, item 5; Fig. 2, item 5; col. 3, lines 57 – 62; col. 6, lines 3 - 16); and

a second instruction decoder for decoding program instruction words of a second instruction set (Fig. 1A, item 5; Fig. 2, item 5; col. 3, lines 57 – 62; col. 6, lines 3 - 16);

and in which said processor core controller is operable to control either said first instruction decoder or said second instruction decoder to decode a current program instruction word (Fig. 1A, item 5; Fig. 2, item 5; col. 3, lines 57 – 62; col. 6, lines 3 - 16).

3.3 Regarding claim 3, Larsen discloses program instruction words of said first instruction set are X-bit program instruction words (Abstract; Fig. 2; col. 6, lines 41 - 66); and

program instruction words of said second instruction set are Y-bit program instruction words (Abstract; Fig. 2; col. 6, lines 41 - 66);

Y being different to X (Abstract; Fig. 2; col. 6, lines 41 - 66).

3.4 Per claim 4, the rejection of claim 3 under 35 USC 102(b) (paragraph 3.3 above) applies fully.

3.5 Regarding claims 5 and 6, Larsen discloses that Y is 16. (Abstract; Fig. 2; col. 6, lines 41 – 66 "execute also 'type 2' format or language instructions that arbitrarily utilize **16 bit words** ...").
However, Larsen does not explicitly disclose that X is a **32 bit** instruction word.
Larsen does teach "**let us suppose** that a 'type 1' format or language instruction set requires **24 bit words** ..." (col. 6, lines 41 – 42).
Clearly, it would have been inherent for the 24 bit word example chosen in Larsen to be substituted with a 32 bit word example.

3.6 Per claim 7 , Larsen teaches that said one or more indicator bits of said program counter register are one or more most significant bits of said program counter register (see details of the rejection of claim 1, item (d) above).

3.7 Regarding claim 8, Larsen teaches that said one or more indicator bits of said program counter register are one or more least significant bits of said program counter register (see details of the rejection of claim 1, item (d) above).

3.8 Per claims 9 - 13, Larsen discloses that said one or more indicator bits of said program counter register are one or more least significant bits of said program counter register (see details of the rejection of claim 1, item (d) above).

3.9 Regarding claim 14, Larsen teaches a data memory for storing program instruction words to be executed (Fig. 2, item 4; col. 3, lines 62 – 64 "The execution register 4, abbreviated EXR, contains decoded instructions which are the execution process codes for the specific machine."; col. 7, lines 15 - 22).

3.10 Per claim 65, Larsen teaches a program counter register comprising:

an ordered set of bits (Fig. 1A, item 3; Fig. 2, item 3; col. 3, lines 55 - 64);

wherein a subset of the ordered set of bits identifies an address of an instruction (Fig. 2, items 2, 3; col. 5, line 52 – col. 6, line 2); and at least one bit of the ordered set of bits identifies an instruction set (Fig. 2, items 2, 3; col. 5, line 52 – col. 6, line 2); and

wherein the at least one bit is not a member of the subset (Fig. 2, items 2, 3; col. 5, line 52 – col. 6, line 2).

3.11 Regarding claim 66, Larsen discloses a method of selecting an instruction set comprising the steps of:

receiving a branching instruction written in a first instruction set of a plurality of instruction sets (Fig. 2; col. 5, line 34 – col. 6, line 2; col. 7, lines 12 - 37);

pursuant to the branching instruction, inserting the address of a next instruction into a register and setting the value of a flag, where the value of the flag is not dependent upon the address of the next instruction (Fig. 2; col. 7, lines 12 - 37);

selecting an instruction set based upon the value of the flag (Fig. 2; col. 7, lines 12 - 37); and

acquiring the next instruction at the address inserted into the register (Fig. 2; col. 7, lines 12 - 37).

3.12 Per claim 67, Larsen teaches a processing apparatus comprising:

a pointer for identifying an address of a next instruction that is written in a first instruction set of a plurality of instruction sets (Fig. 2; col. 7, lines 12 - 37); and

a flag for identifying the first instruction set (Fig. 2; col. 7, lines 12 - 37);

wherein:

the pointer and the flag are both written in response to an instruction from a second instruction set of the plurality of instruction sets (Fig. 2; col. 7, lines 12 - 37), and

the value of the flag is not dependent upon the address of the next instruction (Fig. 2; col. 7, lines 12 - 37).

3.13 Regarding claim 68, Larsen discloses the apparatus of claim 67 wherein:

the first instruction set is different from the second instruction set (Abstract; Fig. 2).

3.14 Per claim 69, Larsen teaches the apparatus of claim 67 wherein:

the pointer and the flag are located in a single register (Fig. 2; col. 7, lines 12 - 37).

3.15 Regarding claim 70, Larsen discloses the apparatus of claim 67 wherein:

the pointer and the flag are not located in a single register, yet are written to as if portions of a single register (Fig. 2; col. 7, lines 12 - 37).

3.16 Regarding claims 15 – 64, the rejection of claims 1 – 14 and 65 - 70 under 35 USC 102(b) (paragraphs 3.1 – 3.15 above) applies.

In addition, Larsen discloses setting one or more control flags to indicate that a current instruction set for the data processing apparatus is the instruction set identified based on the instruction set indicator portion of the sequence of bits (Fig. 2; col. 7, lines 12 - 37).

Response to Arguments

4. Applicant's arguments with respect to claims 1 - 70 have been considered but are moot in view of the new ground(s) of rejection.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth R. Coulter whose telephone number is 571 272-3879. The examiner can normally be reached on 5 4 9.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rupal Dharia can be reached on 571 272-3880. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KENNETH R. COULTER
PRIMARY EXAMINER

krc